36-V, 1-A, 4.17-μV_{RMS}, RF LDO Voltage Regulator

FEATURES

- **Input Voltage Range: +3 V to +36 V**
- **Output Voltage Noise**
  - **4.17 μV_{RMS} (10 Hz, 100 kHz)**
- **Power-Supply Ripple Rejection:**
  - **82 dB (100 Hz)**
  - **≥ 55 dB (10 Hz, 10 MHz)**
- **ANY-OUT™ (User-Adjustable Output via PCB Layout):**
  - **No External Resistors or Feed-Forward Capacitors Required**
  - **Output Voltage Range: +1.4 V to +20.5 V**
- **Output Current: 1 A**
- **Dropout Voltage: 307 mV at 1 A**
- **CMOS Logic Level-Compatible Enable Pin**
- **Built-In Fixed Current Limit and Thermal Shutdown**
- **Available in High Thermal Performance Package:**
  - **5-mm × 5-mm QFN**
- **Operating Temperature Range: –40°C to +125°C**

APPLICATIONS

- **Voltage-Controlled Oscillators (VCO)**
- **Frequency Synthesizers**
- **Test and Measurement Applications**
- **Medical Applications**
- **RX, TX, and PA Circuitry**
- **Supply Rails for Operational Amplifiers, DACs, ADCs, and Other High-Precision Analog Circuitry**
- **Audio Applications**
- **Post DC/DC Converter Regulation and Ripple Filtering**
- **Industrial Instrumentation**
- **Base Stations and Telecom Infrastructure**
- **+12-V and +24-V Industrial Buses**

DESCRIPTION

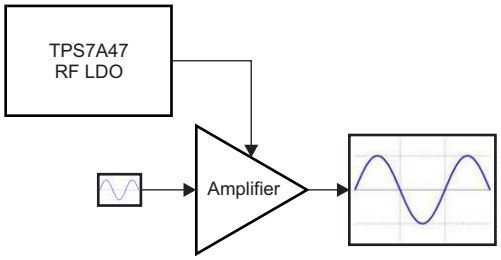
The TPS7A47 is a positive voltage (+36 V), ultralow-noise (4.17 μV_{RMS}) linear regulator capable of sourcing a 1-A load.

In addition, the TPS7A47 output voltage is fully user-adjustable via a printed circuit board (PCB) layout without the need of external resistors or feed-forward capacitors, thus reducing overall component count.

The TPS7A47 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry in critical applications (such as medical, RF, and test-and-measurement).

In addition, the TPS7A47 is ideal for post dc/dc converter regulation. By filtering out the output voltage ripple inherent to dc/dc switching conversions, maximum system performance is ensured in sensitive instrumentation, test-and-measurement, audio, and RF applications.

For applications where positive and negative low-noise rails are required, consider TI's TPS7A33 family of negative high-voltage, ultralow-noise linear regulators.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE
TPS7A4700RGW	VQFN	RGW	–40°C ≤ T_J ≤ +125°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted.(1)

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	IN pin to GND pin	–0.4	+36	V
	EN pin to GND pin	–0.4	+36	V
	EN pin to IN pin	–36	+0.4	V
	OUT pin to GND pin	–0.4	+36	V
	NR pin to GND pin	–0.4	+36	V
	SENSE pin to GND pin	–0.4	+36	V
	0P1V pin to GND pin	–0.4	+36	V
	0P2V pin to GND pin	–0.4	+36	V
	0P4V pin to GND pin	–0.4	+36	V
	0P8V pin to GND pin	–0.4	+36	V
	1P6V pin to GND pin	–0.4	+36	V
	3P2V pin to GND pin	–0.4	+36	V
	6P4V1 pin to GND pin	–0.4	+36	V
	6P4V2 pin to GND pin	–0.4	+36	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	+125	°C
	Storage, T_{stg}	–65	+150	°C
Electrostatic discharge (ESD) ratings(3)	Human body model (HBM) QSS 009-105 (JESD22-A114A)		1000	V
	Charge device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

ELECTRICAL CHARACTERISTICS

At –40°C ≤ T_J ≤ +125°C; V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or V_{IN} = 3.0 V (whichever is greater); V_{EN} = V_{IN}; I_{OUT} = 0 mA; C_{IN} =10 µF; C_{OUT} = 10 µF; C_{NR} = 10 nF; SENSE tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		3		35	V
V_{UVLO}	Under-voltage lockout threshold	V_{IN} rising		2.67		V
		V_{IN} falling		2.5		V
V_{UVLO_HYS}	Under-voltage lockout hysteresis			177		mV
V_{NR}	Noise reduction pin voltage			V_{OUT}		V
V_{OUT}	Output voltage range	V_{IN} ≥ $V_{OUT(NOM)}$ + 1.0 V or 3V (whichever is greater), C_{OUT} = 20 µF	1.4		20.5	V
	Nominal accuracy	T_J = +25°C, C_{OUT} = 20 µF	–1.0		1.0	%V_{OUT}
	Overall accuracy	$V_{OUT(NOM)}$ + 1.0 V ≤ V_{IN} ≤ 35 V, 0 mA ≤ I_{OUT} ≤ 1 A, C_{OUT} = 20 µF	–2.5		2.5	%V_{OUT}
$\Delta V_{OUT}(\Delta V_{IN})/V_{OUT(NOM)}$	Line regulation	$V_{OUT(NOM)}$ + 1.0 V ≤ V_{IN} ≤ 35 V		0.092		%V_{OUT}
$\Delta V_{OUT}(\Delta I_{OUT})/V_{OUT(NOM)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 1 A		0.3		%V_{OUT}
V_{DO}	Dropout voltage	V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 0.5 A		216		mV
		V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 1 A		307	450	mV
I_{CL}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$	1	1.26		A
I_{GND}	Ground pin current	I_{OUT} = 0 mA		0.58	1.0	mA
		I_{OUT} = 1 A		6.1		mA
I_{SHDN}	Shutdown supply current	V_{EN} = 0.4 V		2.55	8	µA
		V_{EN} = 0.4 V, V_{IN} = 35 V		3.04	60	µA
I_{EN}	Enable pin current	V_{EN} = V_{IN}		0.78	2	µA
		V_{IN} = V_{EN} = 35 V		0.81	2	µA
$V_{+EN(HI)}$	Enable high-level voltage		2.0		V_{IN}	V
$V_{+EN(LO)}$	Enable low-level voltage		0.0		0.4	V
V_{NOISE}	Output noise voltage	V_{IN} = 3 V, $V_{OUT(NOM)}$ = 1.4 V, C_{OUT} = 50 µF, C_{NR} = 1 µF, BW = 10 Hz to 100 kHz		4.17		μV_{RMS}
		V_{IN} = 6 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 50 µF, C_{NR} = 1 µF, BW = 10 Hz to 100 kHz		4.67		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = 16 V, $V_{OUT(NOM)}$ = 15 V, C_{OUT} = 50 µF, I_{OUT} = 500 mA, C_{NR} = 1 µF, f = 1 kHz		78		dB
T_J	Operating junction temperature		–40		+125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+170		°C
		Reset, temperature decreasing		+150		°C

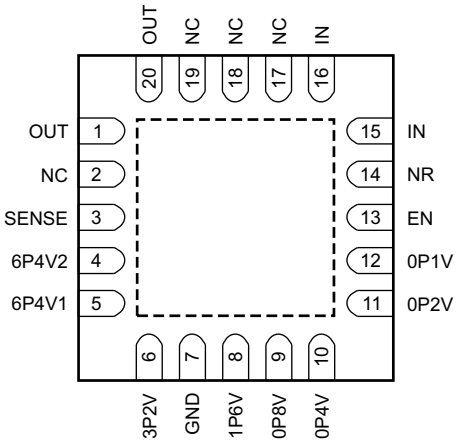
THERMAL INFORMATION

THERMAL METRIC(1)		TPS7A47 RGW 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	32.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	27	
θ_{JB}	Junction-to-board thermal resistance	11.9	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	11.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

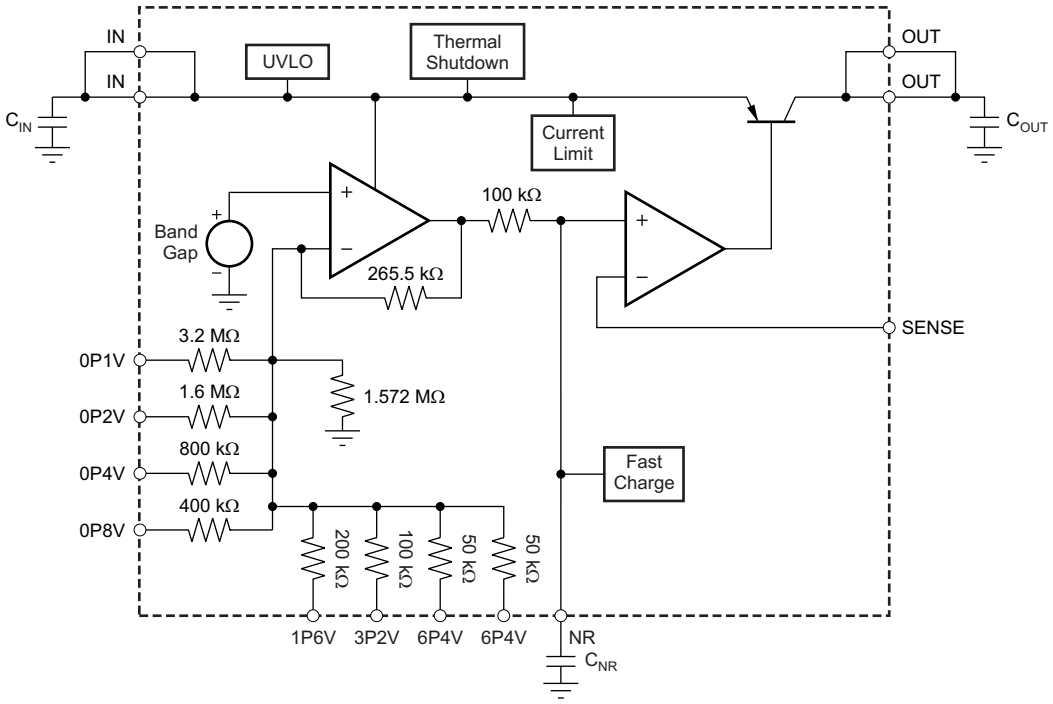
RGW PACKAGE
5-mm × 5-mm QFN-20
(TOP VIEW)



PIN DESCRIPTIONS

PIN		
NAME	**NO.**	**DESCRIPTION**
0P1V	12	When connected to GND, this pin adds 0.1 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P2V	11	When connected to GND, this pin adds 0.2 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P4V	10	When connected to GND, this pin adds 0.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P8V	9	When connected to GND, this pin adds 0.8 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
1P6V	8	When connected to GND, this pin adds 1.6 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
3P2V	6	When connected to GND, this pin adds 3.2 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V1	5	When connected to GND, this pin adds 6.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V2	4	When connected to GND, this pin adds 6.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
EN	13	This pin turns the regulator on and off.
GND	7	Ground
IN	15, 16	Input supply. A capacitor greater than or equal to 1 µF must be tied from this pin to ground to assure stability. A 10-µF capacitor is recommended to be connected from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input traces or high source impedances are encountered.
NC	2, 17-19	This pin can be left open or tied to any voltage between GND and IN.
NR	14	Noise reduction pin. When a capacitor is connected from this pin to GND, RMS noise can be reduced to very low levels. A capacitor greater than or equal to 10 nF must be tied from this pin to ground to assure stability. A 1-µF capacitor is recommended to be connected from NR to GND (as close to the device as possible) to maximize ac performance and minimize noise.
OUT	1, 20	Regulator output. A capacitor greater than or equal to 10 µF must be tied from this pin to ground to assure stability. A 47-µF ceramic output capacitor is highly recommended to be connected from OUT to GND (as close to the device as possible) to maximize ac performance.
SENSE	3	Control-loop error amplifier input. This pin must be connected to OUT. OUT is recommended to be connected at the point of load to maximize accuracy.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At –40°C ≤ T_J ≤ +125°C; V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or V_{IN} = 3.0 V (whichever is greater); V_{EN} = V_{IN}; I_{OUT} = 0 mA; C_{IN} =10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

NOISE vs OUTPUT VOLTAGE

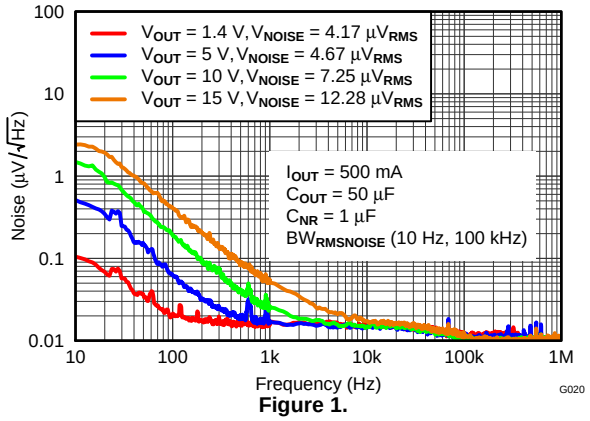


Figure 1.

LINE REGULATION

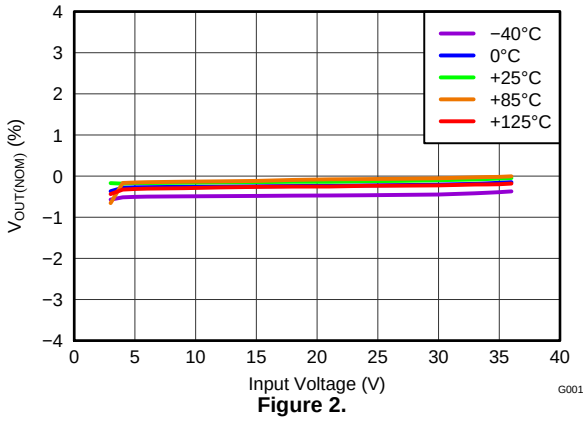


Figure 2.

LOAD REGULATION

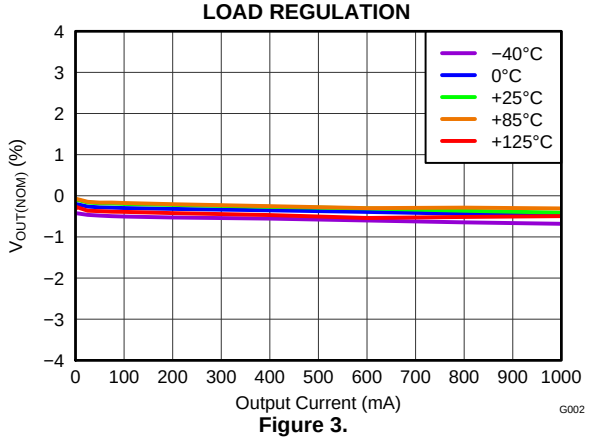


Figure 3.

DROPOUT VOLTAGE vs OUTPUT CURRENT

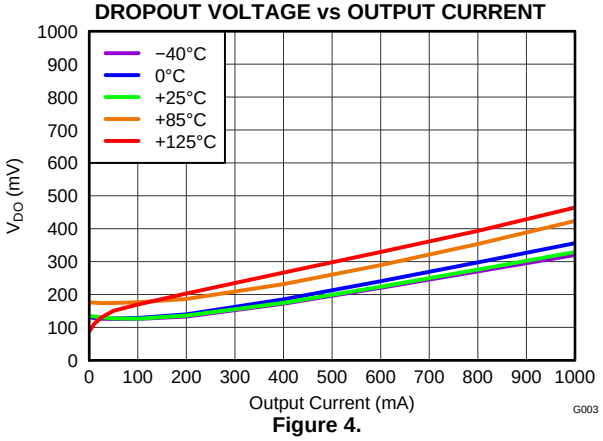


Figure 4.

UVLO THRESHOLD vs TEMPERATURE

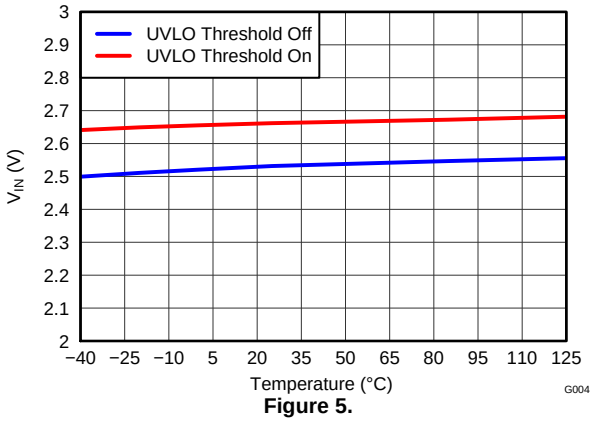


Figure 5.

ENABLE VOLTAGE THRESHOLD vs TEMPERATURE

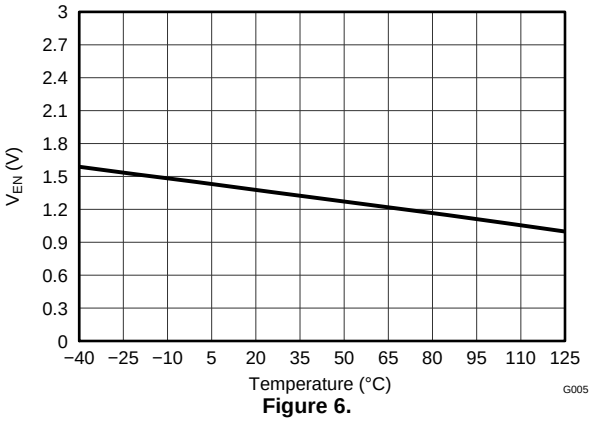


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At –40°C ≤ T_J ≤ +125°C; V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or V_{IN} = 3.0 V (whichever is greater); V_{EN} = V_{IN}; I_{OUT} = 0 mA; C_{IN} =10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

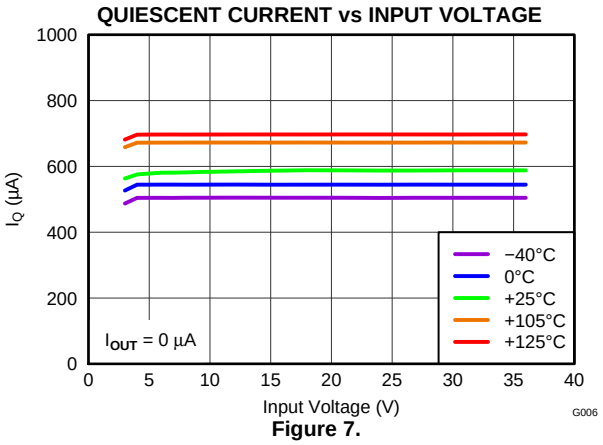


Figure 7.

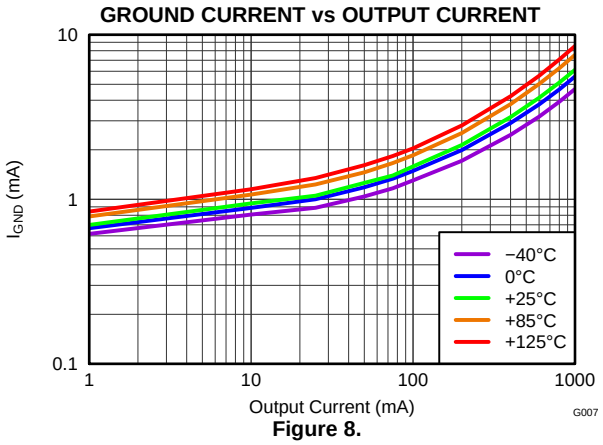


Figure 8.

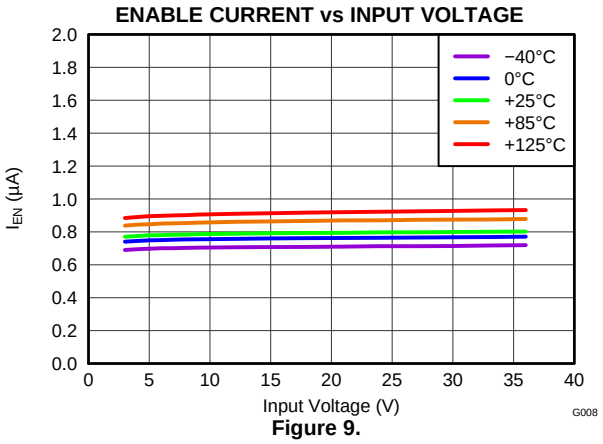


Figure 9.

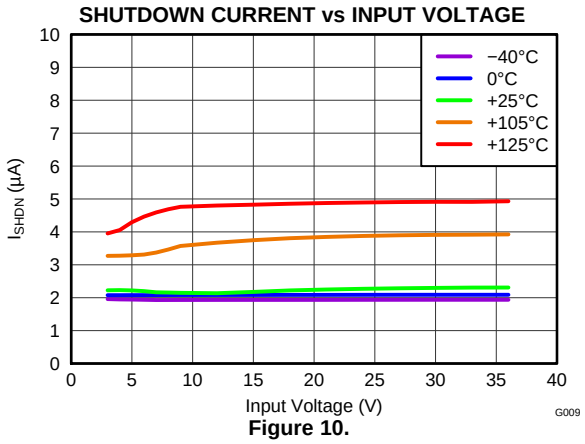


Figure 10.

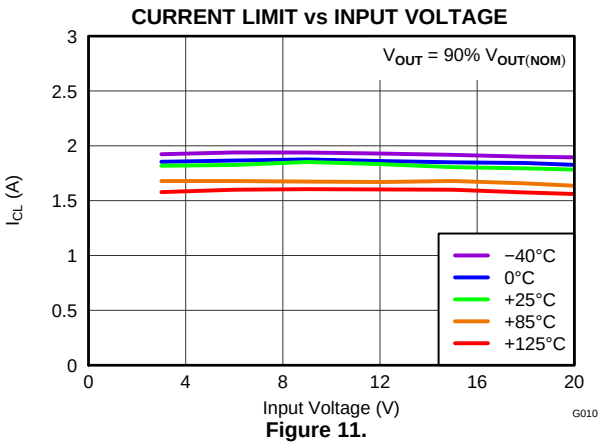


Figure 11.

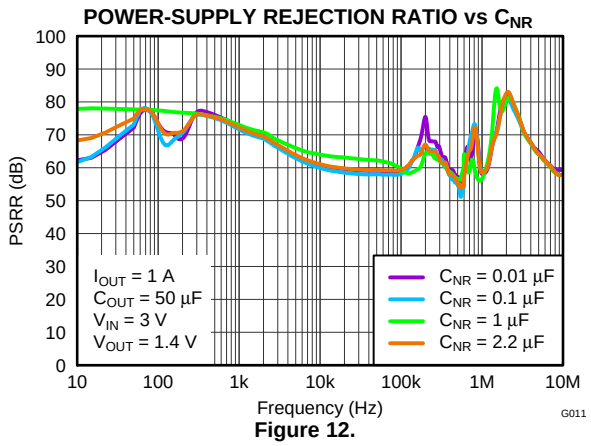


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At –40°C ≤ T_J ≤ +125°C; V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or V_{IN} = 3.0 V (whichever is greater); V_{EN} = V_{IN}; I_{OUT} = 0 mA; C_{IN} =10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

POWER-SUPPLY REJECTION RATIO vs C_{NR}

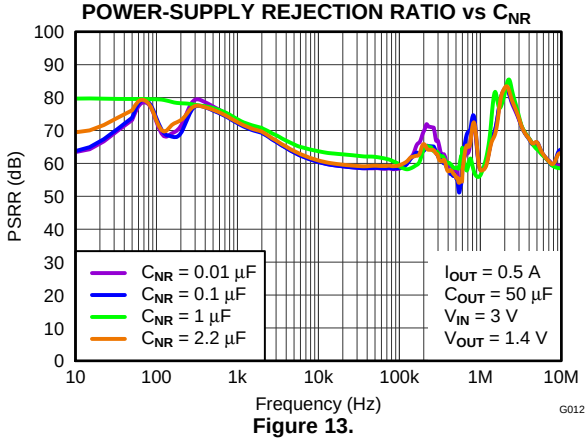


Figure 13.

POWER-SUPPLY REJECTION RATIO vs I_{OUT}

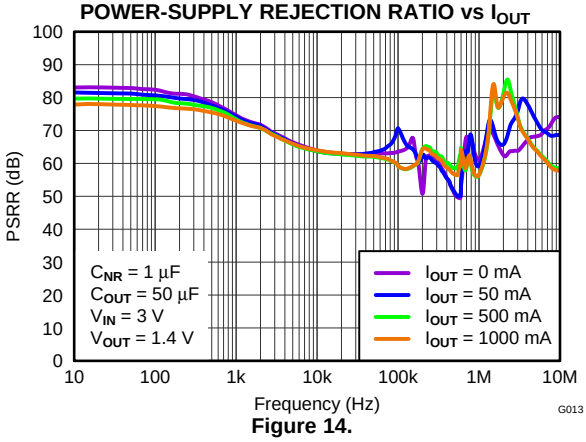


Figure 14.

POWER-SUPPLY REJECTION RATIO vs DROPOUT

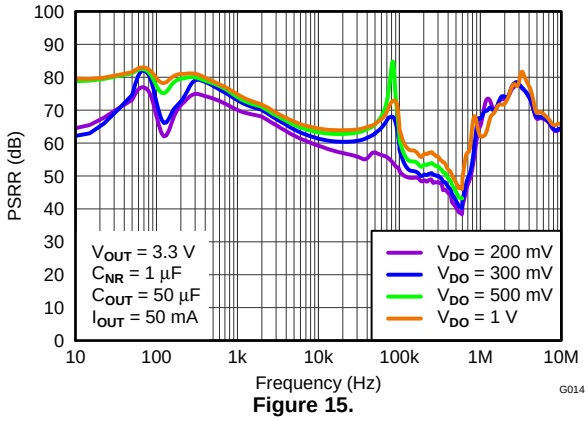


Figure 15.

POWER-SUPPLY REJECTION RATIO vs DROPOUT

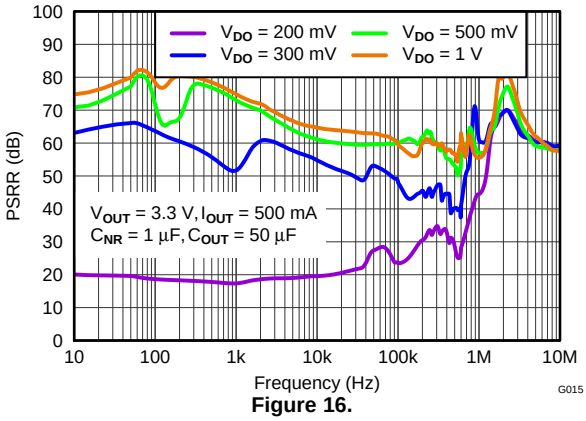


Figure 16.

POWER-SUPPLY REJECTION RATIO vs DROPOUT

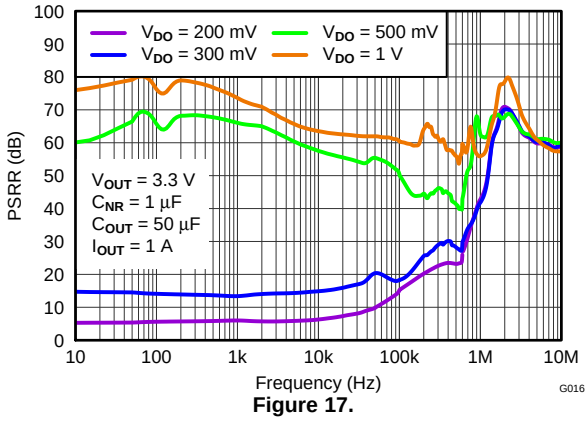


Figure 17.

POWER-SUPPLY REJECTION RATIO vs OUTPUT VOLTAGE

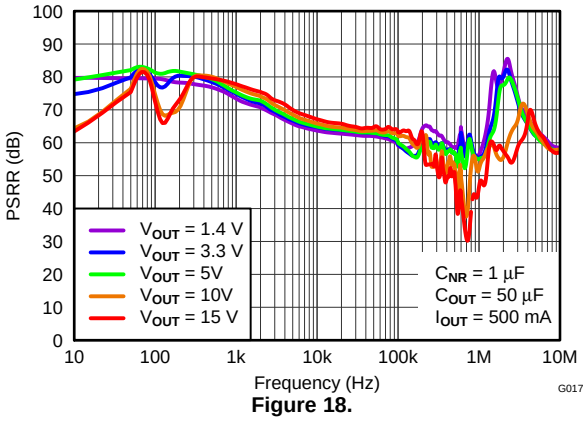


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At –40°C ≤ T_J ≤ +125°C; V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or V_{IN} = 3.0 V (whichever is greater); V_{EN} = V_{IN}; I_{OUT} = 0 mA; C_{IN} =10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

POWER-SUPPLY REJECTION RATIO vs OUTPUT VOLTAGE

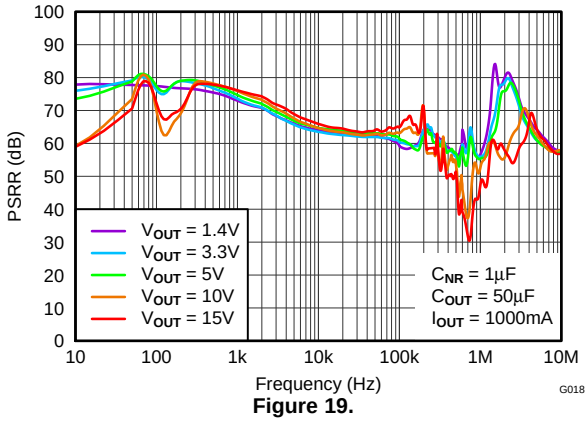


Figure 19.

LOAD TRANSIENT

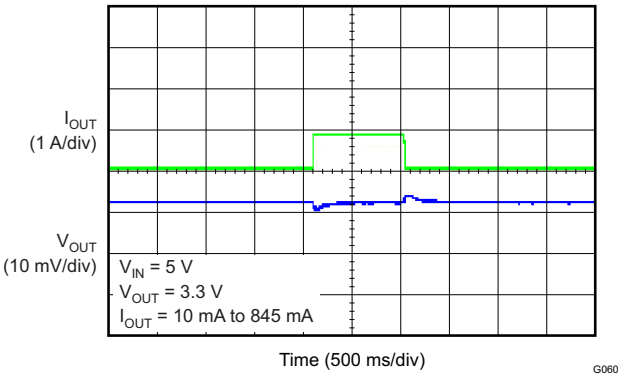


Figure 20.

LINE TRANSIENT

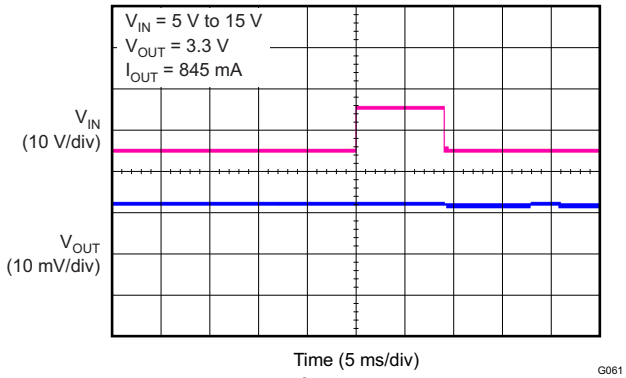


Figure 21.

STARTUP

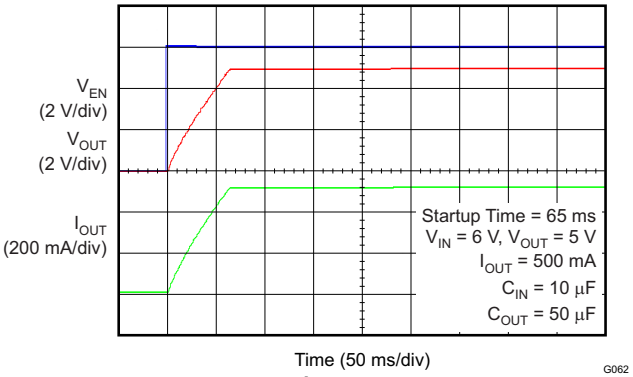


Figure 22.

NOISE vs OUTPUT CURRENT

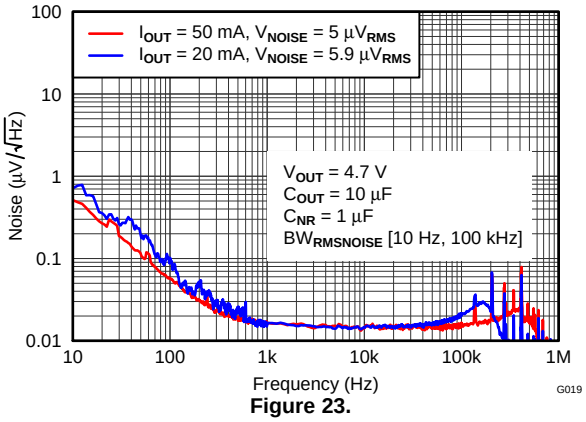


Figure 23.

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUIT

Output voltage is set by grounding the appropriate control pins, as shown in Figure 24. When grounded, all control pins add a specific voltage on top of the internal reference voltage (V_{REF} = 1.4 V). For example, when grounding pins 0P1V, 0P2V, and 1P6V, the voltage values 0.1 V, 0.2 V, and 1.6 V are added to the 1.4-V internal reference voltage for $V_{OUT(NOM)}$ equal to 3.3 V, as described in Equation 1.

$$V_{OUT(NOM)} = V_{REF} + 0.1\ V + 0.2\ V + 1.6\ V = 1.4\ V + 0.1\ V + 0.2\ V + 1.6\ V = 3.3\ V \quad (1)$$

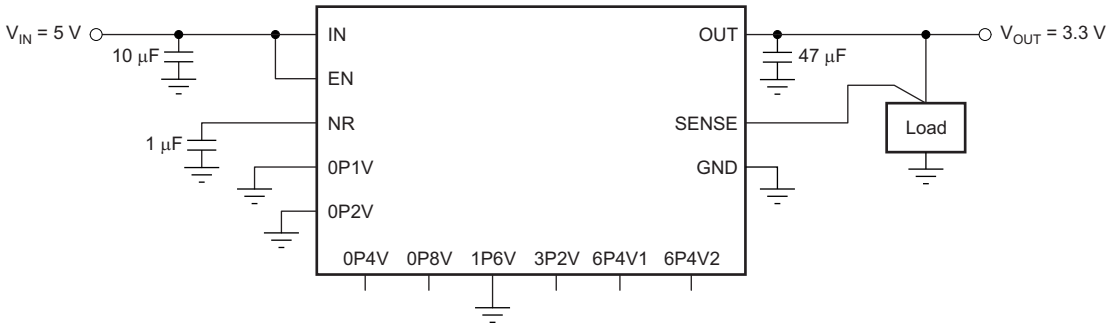


Figure 24. Maximize PSRR Performance and Minimize RMS Noise

ANY-OUT PROGRAMMABLE OUTPUT VOLTAGE

The TPS7A4700 does not use external resistors to set output voltage, as is typical of low-dropout regulators (LDOs), but uses device pins 4, 5, 6, 8, 9, 10, 11, and 12 to program the regulated output voltage. Each pin is either connected to ground (active) or is left open, or floating, (inactive). The ANY-OUT programming is set by Equation 2 as the sum of the internal reference voltage (V_{REF} = 1.4 V) plus the accumulated sum of the respective voltages assigned to each active pin. That is, 100 mV (pin 12), 200 mV (pin 11), 400 mV (pin 10), 800 mV (pin 9), 1.6 V (pin 8), 3.2 V (pin 6), 6.4 V (pin 5), or 6.4 V (pin 4). Table 1 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{REF}.

$$V_{OUT} = V_{REF} + (\Sigma\ \text{ANY-OUT Pins to Ground}) \quad (2)$$

Table 1. ANY-OUT Programmable Output Voltage

ANY-OUT PROGRAM PINS (Active Low)	ADDITIVE OUTPUT VOLTAGE LEVEL
Pin 4 (6P4V2)	6.4 V
Pin 5 (6P4V1)	6.4 V
Pin 6 (3P2)	3.2 V
Pin 8 (1P6)	1.6 V
Pin 9 (0P8)	800 mV
Pin 10 (0P4)	400 mV
Pin 11 (0P2)	200 mV
Pin 12 (0P1)	100 mV

There are several alternative ways to set the output voltage. The program pins can be driven using external general-purpose input/output pins (GPIOs), manually connected to ground using 0-Ω resistors (or left open), or hardwired by the given layout of the printed circuit board (PCB) to set the ANY-OUT voltage. The TPS7A4700 evaluation module (EVM), available for download from www.ti.com, allows the output voltage to be programmed using jumpers.

CAPACITOR RECOMMENDATION

The TPS7A4700 is designed to be stable using low equivalent series resistance (ESR), ceramic capacitors at the input, output, and at the noise reduction pin (NR, pin 14). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended here, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature whereas the use of Y5V-rated capacitors is discouraged precisely because the capacitance varies so widely. In all cases, ceramic capacitance varies a great deal with operating voltage and the design engineer should be aware of these characteristics. As a rule of thumb, ceramic capacitors are recommended to be derated by 50%. The input and output capacitors recommended herein account for a capacitance derating of 50%.

Attention should be given to the input capacitance to minimize transient input droop during load current steps because the TPS7A4700 has a very fast load transient response. Large input capacitances (greater than 10 µF) have a good effect and do not affect stability. Note however that simply using large ceramic input capacitances can also cause unwanted ringing at the output if the input capacitor, in combination with the wire lead inductance, creates a high-Q peaking effect during transients. For example, a 5-nH lead inductance and a 10-µF input capacitor form an LC filter with a resonance frequency of 712 kHz at the edge of the control loop bandwidth. Short, well-designed interconnect leads to the up-stream supply minimize this effect without adding damping. Damping of unwanted ringing can be accomplished by using a tantalum capacitor, with a few hundred milliohms of ESR, in parallel with the ceramic input capacitor.

Input and Output Capacitor Requirements

The TPS7A4700 is designed and characterized for operation with ceramic capacitors of 10 µF or greater at the input and output. Optimal noise performance is characterized using a total output capacitor value of 50 µF. Note especially that input and output capacitances should be located as near as practical to the respective input and output pins.

Noise Reduction Capacitor (C_{NR})

The noise reduction capacitor, connected to the NR pin of the LDO, forms an RC filter for filtering out noise that might ordinarily be amplified by the control loop and appear on the output voltage. Larger capacitances, up to 1 µF, affect noise reduction at lower frequencies while also tending to further reduce noise at higher frequencies. Note that C_{NR} also serves a secondary purpose in programming the turn-on rise time of the output voltage and thereby controls the turn-on surge current.

INTERNAL CURRENT LIMIT (I_{CL})

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate at a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls while load impedance decreases. Note also that when a current limit occurs while the resulting output voltage is low, excessive power may be dissipated across the LDO, which results in a thermal shutdown of the output.

DROPOUT VOLTAGE (V_{DO})

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$). However, in the Electrical Characteristics V_{DO} is defined as the $V_{IN} – V_{OUT}$ voltage at the rated current (I_{RATED}), where the main current pass-FET is fully on in the Ohmic region of operation and is characterized by the classic $R_{DS(ON)}$ of the FET. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. If the input falls below this V_{DO} limit ($V_{IN} < V_{OUT} + V_{DO}$), then the output voltage decreases in order to follow the input voltage.

Dropout voltage is always determined by the $R_{DS(ON)}$ of the main pass-FET. Therefore, if the LDO operates below the rated current, then the V_{DO} for that current scales accordingly. The $R_{DS(ON)}$ for the TPS7A4700 can be calculated using Equation 3.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (3)$$

OUTPUT VOLTAGE ACCURACY

The output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. This accuracy error typically includes the errors introduced by the internal reference and the load and line regulation across the full range of rated load and line operating conditions over temperature, unless otherwise specified by the Electrical Characteristics. Output voltage accuracy also accounts for all variations between manufacturing lots.

STARTUP

Enable (EN) and Under-Voltage Lockout (UVLO)

The TPS7A4700 only turns on when both EN and UVLO are above the respective voltage thresholds. The UVLO circuit monitors input voltage (V_{IN}) to prevent device turn-on before V_{IN} rises above the lockout voltage. The UVLO circuit also causes a shutdown when V_{IN} falls below lockout. The EN signal allows independent logic-level turn-on and shutdown of the LDO when the input voltage is present. EN can be connected directly to V_{IN} if independent turn-on is not needed.

Soft-Start and Inrush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO have achieved threshold voltage. The noise reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

Inrush current is defined as the current through the LDO from IN to OUT during the time of the turn-on ramp up. Inrush current then consists primarily of the sum of load and charge current to the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, this soft-start current can be estimated by Equation 4:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right]$$

where:

$V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp,
$dV_{OUT}(t)/dt$ is the slope of the V_{OUT} ramp, and
R_{LOAD} is the resistive load impedance. (4)

AC PERFORMANCE

LDO ac performance is typically understood to include power-supply rejection ratio, load step transient response, and output noise. These metrics are primarily a function of open-loop gain and bandwidth, phase margin, and reference noise.

Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of how well the LDO control loop rejects ripple noise from the input source to make the dc output voltage as noise-free as possible across the frequency spectrum (usually 10 Hz to 10 MHz). Even though PSRR is therefore a loss in noise signal amplitude (the output ripple relative to the input ripple), the PSRR reciprocal is plotted in the Electrical Characteristics as a positive number in decibels (dB) for convenience. Equation 5 gives the PSRR calculation as a function of frequency where input noise voltage [$V_{S(IN)}(f)$] and output noise voltage [$V_{S(OUT)}(f)$] are understood to be purely ac signals.

$$PSRR\ (dB) = 20\ Log_{10}\left[\frac{V_{S(IN)}(f)}{V_{S(OUT)}(f)}\right] \quad (5)$$

Noise that couples from the input to the internal reference voltage for the control loop is also a primary contributor to reduced PSRR magnitude and bandwidth. This reference noise is greatly filtered by the noise reduction capacitor at the NR pin of the LDO in combination with an internal filter resistor (R_{SS}) for optimal PSRR.

The LDO is often employed not only as a dc/dc regulator, but also to provide exceptionally clean power-supply voltages that are free of noise and ripple to power-sensitive system components. This usage is especially true for the TPS7A4700.

Load Step Transient Response

The load step transient response is the output voltage response by the LDO to a step change in load current whereby output voltage regulation is maintained. The worst-case response is characterized for a load step of 10 mA to 1 A (at 1 A per microsecond) and shows a classic critically-damped response of a very stable system. The voltage response shows a small dip in the output voltage when charge is initially depleted from the output capacitor and then the output recovers as the control loop adjusts itself. The depth of the charge depletion immediately after the load step is directly proportional to the amount of output capacitance. However, to some extent, the speed of recovery is inversely proportional to that same output capacitance. In other words, larger output capacitances act to decrease any voltage dip or peak occurring during a load step but also decrease the control-loop bandwidth, thereby slowing response.

The worst-case off-loading step characterization occurs when the current step transitions from 1 A to 0 mA. Initially, the LDO loop cannot respond fast enough to prevent a small increase in output voltage charge on the output capacitor. Because the LDO cannot sink charge current, the control loop must turn off the main pass-FET to wait for the charge to deplete, thus giving the off-load step its typical monotonic decay (which appears triangular in shape).

Noise

The TPS7A4700 is designed, in particular, for system applications where minimizing noise on the power-supply rail is critical to system performance. This scenario is the case for phase-locked loop (PLL)-based clocking circuits for instance, where minimum phase noise is all important, or in-test and measurement systems where even small power-supply noise fluctuations can distort instantaneous measurement accuracy. Because the TPS7A4700 is also designed for higher voltage industrial applications, the noise characteristic is well designed to minimize any increase as a function of the output voltage.

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits alone. This noise is the sum of various types of noise (such as shot noise associated with current-through-pin junctions, thermal noise caused by thermal agitation of charge carriers, flicker noise or 1/f noise that is a property of resistors and dominates at lower frequencies as a function of 1/f, burst noise, and avalanche noise).

To calculate the LDO RMS output noise, a spectrum analyzer must first measure the spectral noise across the bandwidth of choice (typically 10 Hz to 100 kHz in units of $\mu V/\sqrt{Hz}$). The RMS noise is then calculated in the usual manner as the integrated square root of the squared spectral noise over the band, then averaged by the bandwidth.

THERMAL INFORMATION

Thermal Protection

The TPS7A4700 contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. Thermal shutdown occurs when the thermal junction temperature (T_J) of the main pass-FET exceeds +170°C (typical). Thermal shutdown hysteresis assures that the LDO again resets (turns on) when the temperature falls to +150°C (typical). Because the TPS7A4700 is capable of supporting high input voltages, a great deal of power can be expected to be dissipated across the device at low output voltages which may cause a thermal shutdown. The thermal time-constant of the semiconductor die is fairly short, and thus the output oscillates on and off at a high rate when thermal shutdown is reached until power dissipation is reduced.

For reliable operation, the junction temperature should be limited to a maximum of +125°C. To estimate the thermal margin in a given layout, increase the ambient temperature until the thermal protection shutdown is triggered using worst-case load and highest input voltage conditions. For good reliability, thermal shutdown should occur at least +45°C above the maximum expected ambient temperature condition for the application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A4700 is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A4700 into thermal shutdown degrades device reliability.

Power Dissipation (P_D)

Circuit reliability demands that due consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and proper sizing of the thermal plane. The PCB area around the regulator should be as free as possible of other heat-generating devices that can cause added thermal stresses.

Power dissipation in the regulator depends on the input to output voltage difference and load conditions. P_D can be calculated using Equation 6:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \quad (6)$$

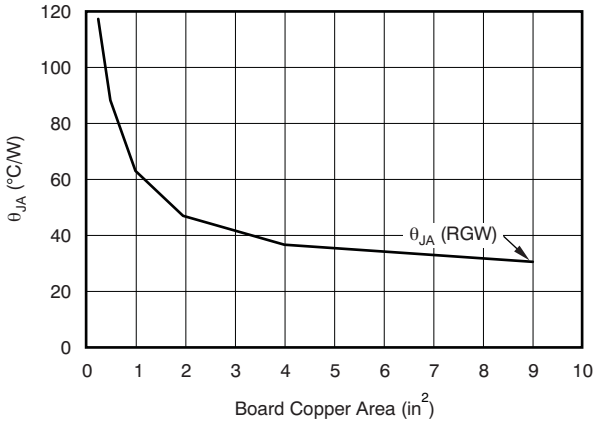
It is important to note that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input voltage necessary for output regulation to be obtained.

The primary heat conduction path for the QFN (RGW) package is through the thermal pad to the PCB. The thermal pad should be soldered to a copper pad area under the device. This pad area should then contain an array of plated vias that conduct heat to any inner spreading plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 7.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (7)$$

Unfortunately, this thermal resistance (θ_{JA}) is highly dependant on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the spreading planes. The θ_{JA} recorded in the Thermal Information table is determined by the JEDEC standard, PCB, and copper-spreading area and is to be used only as a relative measure of package thermal performance. Note that for a well-designed thermal layout, θ_{JA} is actually the sum of the QFN package junction-to-case (bottom) thermal resistance (θ_{JCbot}) plus the thermal resistance contribution by the PCB copper. By knowing θ_{JCbot}, the minimum amount of appropriate heat sinking can be used to estimate θ_{JA} with Figure 25. θ_{JCbot} can be found in the Thermal Information table.



NOTE: θ_{JA} value at a board size of 9-in^2 (that is, 3-in × 3-in) is a JEDEC standard.

Figure 25. θ_{JA} vs Board Size

Estimating Junction Temperature

The JEDEC standard now recommends the use of PSI thermal metrics to estimate the junction temperatures of the LDO while in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These PSI metrics are determined to be significantly independent of copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the Thermal Information table and are used in accordance with Equation 8.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \times P_D$

Ψ_{JB}: $T_J = T_B + \Psi_{JB} \times P_D$

where:

P_D is the power dissipated as explained in Equation 6,

T_T is the temperature at the center-top of the device package, and

T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge. (8)

BOARD LAYOUT

For best overall performance, all circuit components are recommended to be located on the same side of the circuit board and as near as practical to the respective LDO pin connections. Ground return connections to the input and output capacitor, and to the LDO ground pin should also be as close to each other as possible and connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and should be either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the PowerPAD™. In most applications, this ground plane is necessary to meet thermal requirements.

Use the TPS7A4700EVM-094 evaluation module (EVM), available for download at www.ti.com, as a reference for layout and application design.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2012) to Revision A	Page
• Moved to full production data (changes throughout document)	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS7A4700RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS7A4700RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

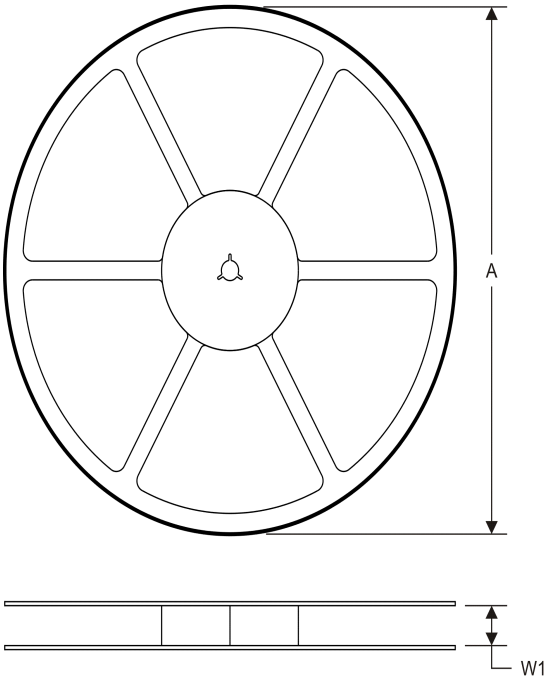
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

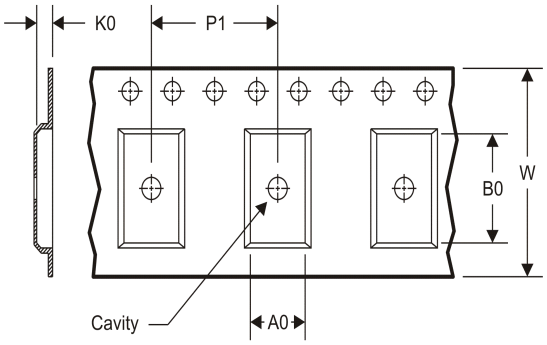
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



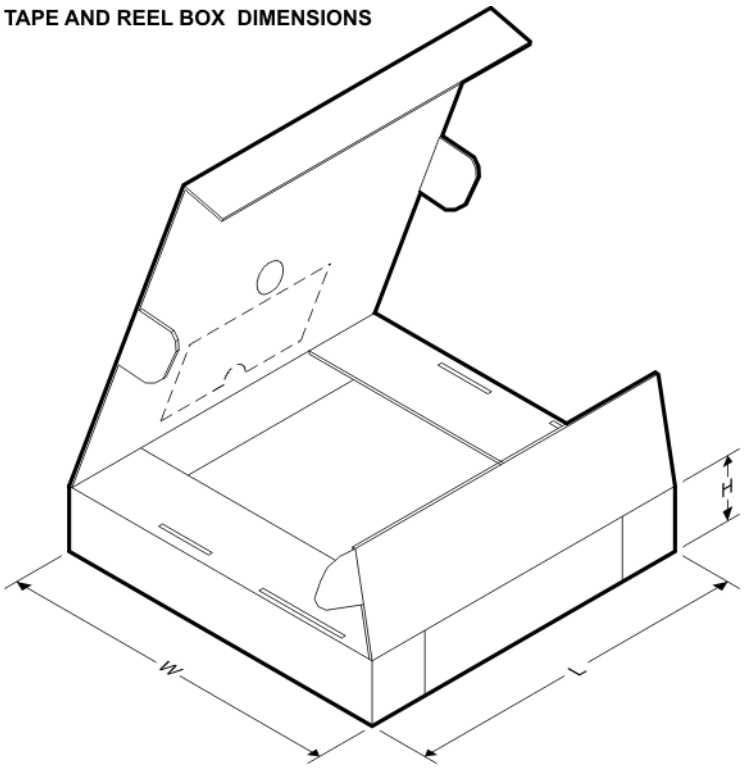
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4700RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS7A4700RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

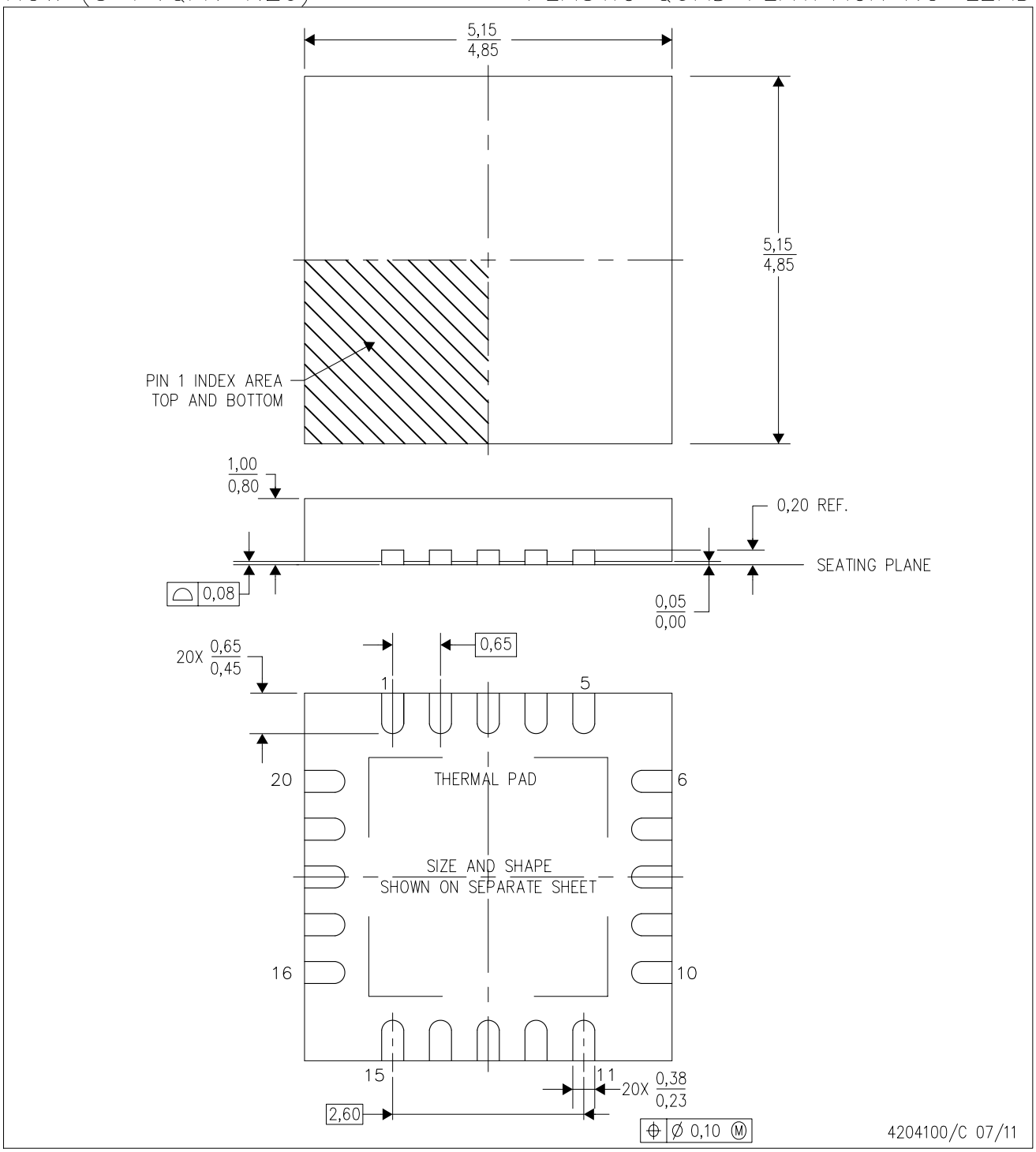
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4700RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS7A4700RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

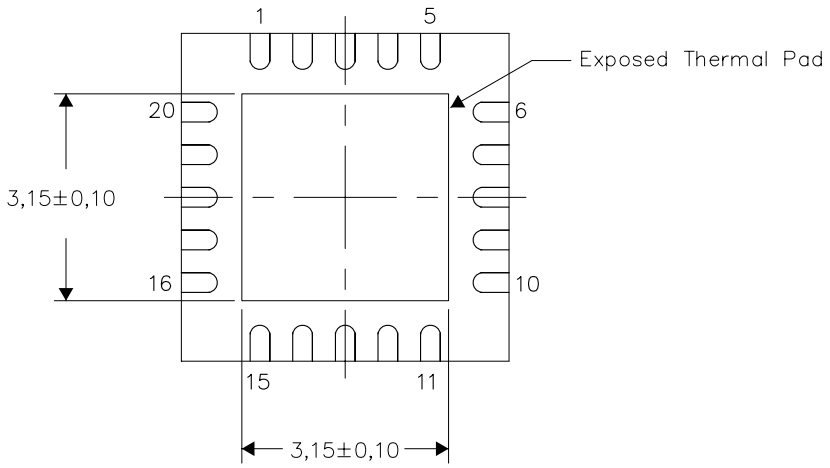
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



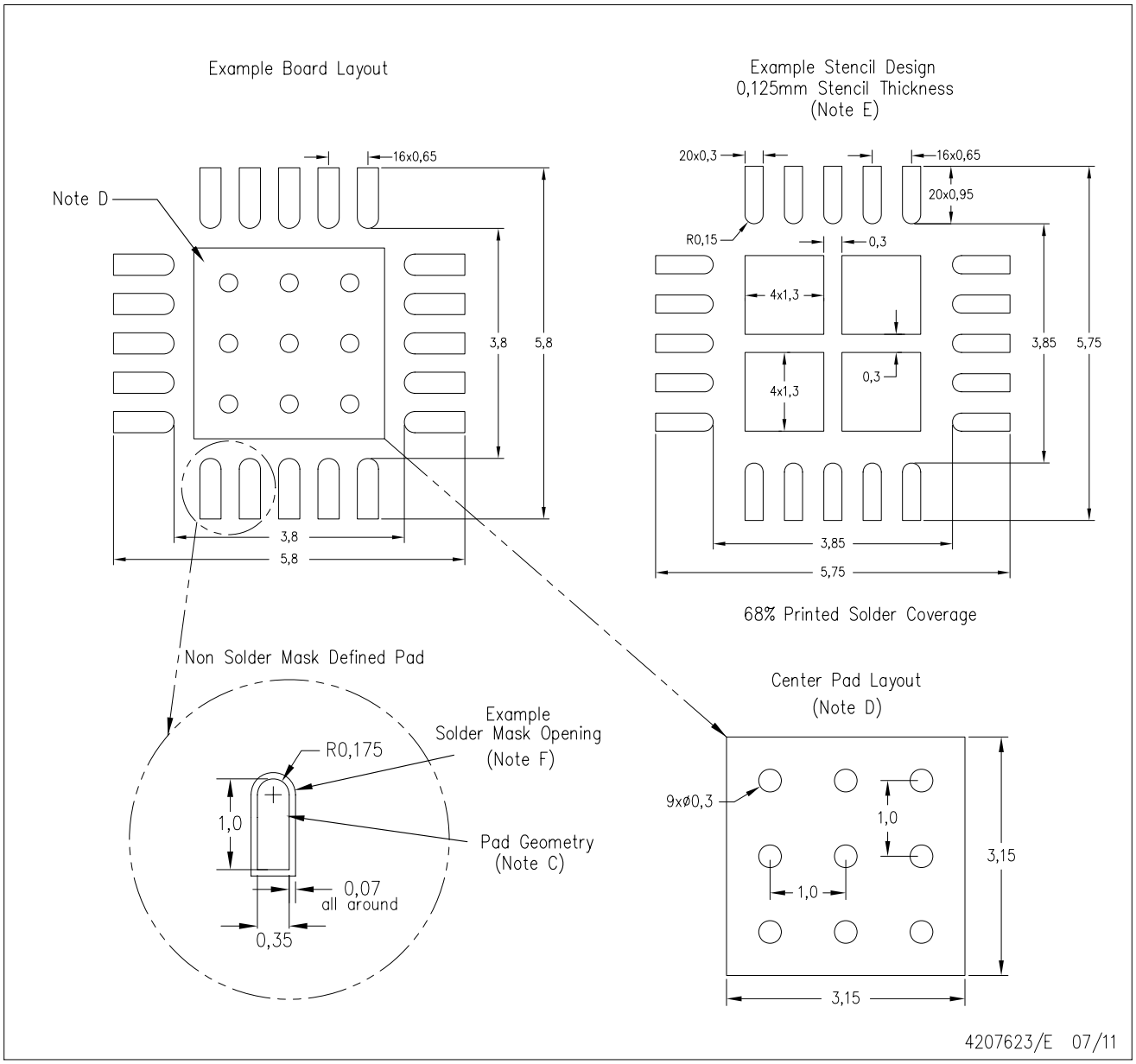
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/J 07/11

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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